

WE CLAIM:

1. A multiport memory, comprising:

    a plurality of RAMs; and

    a port expansion unit connected to access ports of  
    said plurality of RAMs;

        said port expansion unit including,

            an input circuit which allows access control  
            information for activating said plurality of RAMs in  
            parallel every memory cycles to be collectively inputted  
            thereto by a plurality of memory cycles;

        a timing generator which generates internal  
        clock signals capable of prescribing said each memory  
        cycle serially plural times during one cycle of a clock  
        signal supplied from the outside; and

        a logic circuit capable of sequentially  
        supplying the access control information of said input  
        circuit to said plurality of RAMs in parallel in parts  
        every serial memory cycles synchronized with said each  
        internal clock signal.

2. The multiport memory according to claim 1,  
wherein said each RAM is a single port RAM which  
incorporates therein memory cells each having a data  
input/output terminal and a selection terminal as one  
pair,

    said input circuit has read address input circuits,

write address input circuits and write data input circuits corresponding to numbers respectively equal to the number of said signal port RAMs,

    said write address input circuits have latches which latch write addresses therein, respectively,

    said write data input circuits have latches which latch write data therein, respectively, and

    said logic circuit supplies address signals of said each individual read address input circuits to their corresponding single-port RAMs in parallel in synchronism with one internal clock signal for each cycle of the clock signal supplied from the outside to thereby allow a read operation, and supplies write addresses and write data latched in said latches provided every said write address and write data input circuits to said single-port RAMs in parallel in synchronism with other internal clock signals sequentially to thereby permit a write operation on a serial basis plural times.

3. The multiport memory according to claim 1, wherein said each RAM is a two-port RAM which incorporates therein memory cells each having data input/output terminals and selection terminals as two pairs and which has two ports capable of parallel access from the outside,

    said input circuit has read address input circuits, write address input circuits and write data input

circuits corresponding to numbers respectively equal to the number of said two-port RAMs,

    said write address input circuits have a latch which latches write addresses therein,

    said write data input circuits have a latch which latches write data therein, and

    said logic circuit supplies address signals of said each individual read address input circuits to one ports of their corresponding two-port RAMs in parallel in synchronism with one internal clock signal for each cycle of the clock signal supplied from the outside to thereby allow a read operation, supplies write addresses and write data latched in said latches in said one write address and write data input circuits to the other ports of all the two-port RAMs in parallel to thereby permit a write operation, and supplies write addresses and write data latched in said latches of other write address and write data input circuits to all the two-port RAMs in parallel in synchronism with another internal clock signal to thereby allow a write operation.

4. The multiport memory according to claim 1, wherein said respective RAM are n two-port RAMs which incorporate therein memory cells each having data input/output terminals and selection terminals as two pairs and each of which has two ports capable of parallel access from the outside,

said input circuit has address input circuits, write data input circuits and read/write signal input circuits in association with the respective ports of said two-port RAMs,

    said address input circuits have latches which latch addresses therein, respectively,

    said write data input circuits have latches which latch write data therein, respectively,

    said read/write signal input circuits have latches which latch read/write signals therein, respectively,

    said timing generator generates mutually non-overlapped first through nth internal clock signals as the internal clock signals, and

    said logic circuit supplies address signals of said each individual address input circuits to which a read operation is specified, to their corresponding ports of said two-port RAMs in parallel in synchronism with the first internal clock signal for each cycle of the clock signal supplied from the outside to thereby allow the read operation, and supplies write addresses and write data latched in said latches in said address and write data input circuits to which a write operation is specified, to all the two-port RAMs in synchronism with the first through nth internal clock signals sequentially to thereby permit the write operation.

5. The multiport memory according to claim 1,

wherein said respective RAMs are n two-port RAMs which respectively incorporate therein memory cells having data input/output terminals and selection terminals as two pairs and each of which has two ports capable of parallel access from the outside,

    said input circuit has read address input circuits, write address input circuits and write data input circuits respectively provided as  $2n$ ,

    said write address input circuits have latches which latch write addresses therein, respectively,

    said write data input circuits have latches which latch write data therein, respectively,

    said timing generator generates mutually non-overlapped first through  $n+1$ th internal clock signals as the internal clock signals, and

    said logic circuit supplies address signals of said each individual read address input circuits to their corresponding two-port RAMs in parallel in synchronism with the first internal clock signal for each cycle of the clock signal supplied from the outside to thereby allow all the RAMs to perform the operation of reading separate data in parallel, and supplies write addresses and write data latched in said latches in said write address and write data input circuits to all the two-port RAMs in order in synchronism with the second through  $n+1$ th internal clock signals sequentially to thereby allow all the RAMs to perform the operation of

sequentially writing the same data.

6. The multiport memory according to any of claims 1 to 5, wherein said each RAM prescribes each memory cycle in synchronism with the clock signal and said timing generator sets the internal clock signals as mutually non-overlapped clock signals and supplies a signal indicative of the OR of their non-overlapped internal clock signals to said each RAM as an enable clock signal.

7. The multiport memory according to claim 6, wherein said logic circuit allows a read operation to said each RAM to take precedence over a write operation during a cycle prescribed by the external clock signal.

8. The multiport memory according to claim 7, which is formed in a single semiconductor chip.

9. A data processor, comprising:  
a CPU; and  
a port expansion circuit;  
said CPU and said port expansion circuit being formed in a semiconductor chip,  
said port expansion circuit being connected to said CPU via an internal bus and connected to access ports of a plurality of RAMs provided outside said semiconductor

chip, thereby allowing access to the access ports with said plurality of RAMs being apparently defined as a single multiport memory, said port expansion circuit including,

an input circuit which allows access control information for operating said plurality of RAMs in parallel every memory cycles to be collectively inputted thereto by a plurality of memory cycles;

a timing generator which generates a control clock signal capable of prescribing said each memory cycle in series plural times during one cycle of a synchronizing clock signal of said data processor; and

a logic circuit capable of sequentially supplying the access control information inputted to said input circuit to said plurality of RAMs in parallel in parts every serial memory cycles synchronized with the control clock signal.

10. A data processing system, comprising:

an access control circuit;

a port expansion circuit; and

a plurality of RAMs;

said port expansion circuit being connected to said access control circuit and access ports of said plurality of RAMs, thereby allowing access to the access ports with said plurality of RAMs being apparently defined as a single multiport memory, said port expansion circuit

including,

an input circuit which allows access control information for operating said plurality of RAMs in parallel every memory cycles to be collectively inputted thereto by a plurality of memory cycles;

a timing generator which generates a control clock signal capable of prescribing said each memory cycle in series plural times during one cycle of a clock signal supplied from the outside; and

a logic circuit capable of sequentially supplying the access control information inputted to said input circuit to said plurality of RAMs in parallel in parts every serial memory cycles synchronized with the control clock signal.

11. The data processing system according to claim 10, wherein said each RAM is a single port RAM which incorporates therein memory cells each having a data input/output terminal and a selection terminal as one pair,

said input circuit has read address input circuits, write address input circuits and write data input circuits corresponding to numbers respectively equal to the number of said signal port RAMs,

said write address input circuits have latches which latch write addresses therein, respectively,

said write data input circuits have latches which

latch write data therein, respectively, and  
said logic circuit supplies address signals of said  
each individual read address input circuits to their  
corresponding single-port RAMs in parallel in synchronism  
with one internal clock signal for each cycle of the  
clock signal supplied from the outside to thereby allow a  
read operation, and supplies write addresses and write  
data latched in said latches provided every said write  
address and write data input circuits to said single-port  
RAMs in parallel in synchronism with other internal clock  
signals sequentially to thereby permit a write operation  
on a serial basis plural times.

12. The data processing system according to claim  
10, wherein said each RAM is a two-port RAM which  
incorporates therein memory cells each having data  
input/output terminals and selection terminals as two  
pairs and which has two ports capable of parallel access  
from the outside,

said input circuit has read address input circuits,  
write address input circuits and write data input  
circuits corresponding to numbers respectively equal to  
the number of said two-port RAMs,

said write address input circuits have a latch  
which latches write addresses therein,

said write data input circuits have a latch which  
latches write data therein, and

said logic circuit supplies address signals of said each individual read address input circuits to one ports of their corresponding two-port RAMs in parallel in synchronism with one internal clock signal for each cycle of the clock signal supplied from the outside to thereby allow a read operation, supplies write addresses and write data latched in said latches in said one write address and write data input circuits to the other ports of all the two-port RAMs in parallel to thereby permit a write operation, and supplies write addresses and write data latched in said latches of other write address and write data input circuits to all the two-port RAMs in parallel in synchronism with another internal clock signal to thereby allow a write operation.

13. The data processing system according to claim 10, wherein said respective RAM are n two-port RAMs which incorporate therein memory cells each having data input/output terminals and selection terminals as two pairs and each of which has two ports capable of parallel access from the outside,

    said input circuit has address input circuits, write data input circuits and read/write signal input circuits in association with the respective ports of said two-port RAMs,

    said address input circuits have latches which latch addresses therein, respectively,

said write data input circuits have latches which latch write data therein, respectively,

    said read/write signal input circuits have latches which latch read/write signals therein, respectively,

    said timing generator generates mutually non-overlapped first through nth internal clock signals as the internal clock signals, and

    said logic circuit supplies address signals of said each individual address input circuits to which a read operation is specified, to their corresponding ports of said two-port RAMs in parallel in synchronism with the first internal clock signal for each cycle of the clock signal supplied from the outside to thereby allow the read operation, and supplies write addresses and write data latched in said latches in said address and write data input circuits to which a write operation is specified, to all the two-port RAMs in synchronism with the first through nth internal clock signals sequentially to thereby permit the write operation.

14. The data processing system according to claim 10, wherein said respective RAMs are n two-port RAMs which respectively incorporate therein memory cells having data input/output terminals and selection terminals as two pairs and each of which has two ports capable of parallel access from the outside,

    said input circuit has read address input circuits,

write address input circuits and write data input circuits respectively provided as  $2^n$ ,

    said write address input circuits have latches which latch write addresses therein, respectively,

    said write data input circuits have latches which latch write data therein, respectively,

    said timing generator generates mutually non-overlapped first through  $n+1$ th internal clock signals as the internal clock signals, and

    said logic circuit supplies address signals of said each individual read address input circuits to their corresponding two-port RAMs in parallel in synchronism with the first internal clock signal for each cycle of the clock signal supplied from the outside to thereby allow all the RAMs to perform the operation of reading separate data in parallel, and supplies write addresses and write data latched in said latches in said write address and write data input circuits to all the two-port RAMs in order in synchronism with the second through  $n+1$ th internal clock signals sequentially to thereby allow all the RAMs to perform the operation of sequentially writing the same data.

15. A semiconductor integrated circuit, comprising:  
    a bus master module activated in synchronism with a first clock signal;  
    a plurality of RAM modules activated in synchronism

with second clock signals having a plurality of phases, which are higher than said first clock signal in frequency; and

a port expansion module which is connected to said bus master module and said plurality of RAM modules and allows said bus master module to be accessed with said plurality of RAM modules as a single multiport memory apparently,

wherein said bus master module allows access control information for activating said plurality of RAM modules in parallel by a plurality of memory cycles to be outputted, and

wherein said port expansion module comprises an input circuit which allows the access control information for operating said plurality of RAM modules in parallel every memory cycles to be collectively inputted by a plurality of memory cycles from said bus master module, a timing generator which generates each second clock signal capable of prescribing said each memory cycle in series plural times during one cycle of the first clock signal, and a logic circuit capable of sequentially supplying the access control information inputted to said input circuit to said plurality of RAM modules in parallel in parts every serial memory cycles synchronized with said each second clock signal.

16. The semiconductor integrated circuit according

to claim 15, wherein said each RAM module prescribes each memory cycle in synchronism with said each second clock signal and said timing generator sets the second clock signals as mutually non-overlapped clock signals and supplies a signal indicative of the OR of their non-overlapped second clock signals to said each RAM module as an enable clock signal.

17. The semiconductor integrated circuit according to claim 15 or 16, wherein said logic circuit allows a read operation to said each RAM module to take precedence over a write operation during a cycle prescribed by an external clock signal.

18. A memory, comprising:

- a plurality of RAMs;
- an input circuit which receives a plurality of pieces of access information for activating said plurality of RAMs therein in parallel in synchronism with a first clock signal; and
- a parallel/serial converter which outputs said plurality of pieces of access information to said plurality of RAMs in series every one or two or more access information,
- wherein said parallel/serial converter performs an output operation in synchronism with a second clock signal higher than the first clock signal in frequency,

and

    said plurality of RAMs are activated in parallel in synchronism with the second clock signal.

19. The memory according to claim 18, wherein a plurality of cycles of the second clock signal are included in one cycle of the first clock signal, and

    a read operation from said each RAM is performed in a first cycle of said plurality of cycles, and a write operation to said each RAM is performed in a second cycle subsequent to the first cycle.

20. The memory according to claim 19, wherein read addresses supplied to said plurality of RAMs are different from one another in said first cycle and write addresses supplied to said plurality of RAMs are common in said second cycle.